CLAIMS

We claim:

1. A chip scale package of an integrated circuit, comprising:

(a) at least one solder ball pad; and

(b) a moat around each solder ball pad.

2. The chip scale package of claim 1, in which at least one passivation layer is disposed on the integrated circuit, and in which the moat is formed in the at least one passivation layer.

3. The chip scale package of claim 2, in which the at least one passivation layer comprises a photo-imageable polymer film.

4. The chip scale package of claim 2, in which the at least one passivation layer has a thickness, and the moat is a full-depth moat having a thickness substantially equal to the thickness of the at least one passivation layer.

5. The chip scale package of claim 4, in which the at least one passivation layer comprises a photo-imageable polymer film.

6. The chip scale package of claim 2, in which the at least one passivation layer has a thickness, and the moat is a partial-depth moat having a thickness of approximately 1-99% of the thickness of the at least one passivation layer.

7. The chip scale package of claim 6, in which the at least one passivation layer comprises a photo-imageable polymer film.

8. The chip scale package of claim 1, in which a first passivation layer is disposed on the integrated circuit, and a second passivation layer, having a thickness, is disposed on the first passivation layer, and in which the moat is formed in the second passivation layer.

9. The chip scale package of claim 8, in which the moat is a full-depth moat having a moat depth substantially equal to the thickness of the second passivation layer.

10. The chip scale package of claim 9, in which at least the second passivation layer comprises a photo-imageable polymer film.

11. The chip scale package of claim 8, in which the moat is a partial-depth moat having a moat depth of approximately 1-99% the thickness of the second passivation layer.

12. The chip scale package of claim 11, in which at least the second passivation layer comprises a photo-imageable polymer film.

13. A wafer for a chip scale package, the wafer having at least one solder ball pad, comprising:

(a) a solder ball at each solder ball pad;

(b) a polymer collar around the solder ball; and

(c) a moat around each solder ball pad.

14. The wafer of claim 13, such that the moat prevents flow of liquefied polymer collar from within the moat to without the moat during and subsequent to heating of the wafer.

15. A method of manufacturing a wafer-level chip scale package, comprising the steps of:

(a) providing a wafer;

(b) disposing a passivation layer on the wafer;

(c) forming in the passivation layer a central feature for a solder ball; and

(d) forming in the passivation layer a moat around the central feature.

16. The method of claim 15, including the steps of

(e) placing a polymer collar within the moat; and

(f) heating the wafer until at least some of the polymer collar liquefies, such that the moat prevents flow of liquefied polymer collar from within the moat to without the moat prior to, and during, curing of the liquid.

17. The method of claim 15, in which the moat is formed by a laser.

18. The method of claim 15, in which the moat is formed by a drill.

19. The method of claim 15, in which the passivation layer comprises a photo-imageable polymer film.

20. The method of claim 15, in which the moat is formed by photo-lithographic means.